6

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,656	01/18/2005	Andrea Giraldo	NL 020650	2185

24737 7590 10/03/2007

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER
PERRY, ANTHONY T

ART UNIT	PAPER NUMBER
2879	

MAIL DATE	DELIVERY MODE
10/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,656	GIRALDO ET AL.	
	Examiner	Art Unit	
	Anthony T. Perry	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 10-12 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). In order to examine the claims on the merits, the Examiner has read claims 10 and 12 as being dependent from claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 7-9, and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Tada et al. (US 2001/0019242).

Regarding claims 1, 2, and 4, Tada et al. disclose an electroluminescent display comprising at least one display pixel, said display pixel comprising at least: a substrate (600); a first electrode (602) deposited on or across said substrate (600); an electroluminescent layer (604), and a second electrode (605) comprising a reflective layer (magnesium-silver alloy) which inherently enhances the light output by reflecting generated light. The display pixel further comprises at least one insulating structure (603) which is part of a dielectric insulating layer deposited across the first electrode (602) and within the display pixel adapted to enhance the light output from said display pixel (for example, see Fig. 6).

Regarding claims 7-9, Tada et al. teach the substrate (600) being thin compared to a lateral dimension of the display pixel and including at least one top substrate layer (601) (for example, see Fig. 6). The Examiner notes that it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation, but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. Regardless, it is noted that the top substrate layer (601) of the Tada reference inherently allows total light reflection for some light output of the display pixel.

Regarding claim 13, Tada et al. teach a method of manufacturing an electroluminescent display comprising at least one display pixel, the method at least comprising the steps of: providing a substrate (600); depositing a first electrode layer (602) on or across said substrate (600); depositing an electroluminescent layer (604) on or across said first electrode layer (602); depositing a second electrode layer (605) on or across said electroluminescent layer (604), characterized in that said method further comprises a structuring step wherein at least one insulating structure (502) is provided within said display pixel adapted to enhance the light output from said display pixel (for example, see Fig. 6)

Regarding claim 14 the structuring step is performed in an insulating layer (603) deposited on or across said first electrode (602) (for example, see paragraph 0073).

Claims 1, 2, 4-11, 13, 14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Goto (US 2002/0063515).

Regarding claims 1, 2, and 4, Goto discloses an electroluminescent display comprising at least one display pixel, said display pixel comprising at least: a substrate (100); a first electrode (109) deposited on or across said substrate (100); an electroluminescent layer (113), and a

second electrode (115) comprising a reflective layer which enhances the light output by reflecting generated light. The display pixel further comprises at least one insulating structure (111) which is part of a dielectric insulating layer deposited on the first electrode (109) and within the display pixel so as to enhance the light output from the display pixel (for example, see Figs. 4(a)-4(b)).

Regarding claims 5-6, Goto teaches the pixel comprising at least one side light output enhancing structure (one of the portions of dielectric layer (111)), which comprises slanted walls (111f) provided to enhance the light output for light generated in the electroluminescent layer (113) of the display pixel and to prevent the light from the pixel from negatively influencing adjacent pixels (for example, see Figs. 4(a)-4(b) and paragraph 0070).

Regarding claims 7-9, Goto teaches the substrate (101) being thin compared to a lateral dimension of the display pixel and including a plurality of top substrate layers (102,104,106) (for example, see Figs. 4(a)-4(b)). The Examiner notes that it has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation, but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. Regardless, it is noted that the top substrate layers (102,104,106) of the Goto reference inherently allow total light reflection for some light output of the display pixel.

Regarding claim 10, Goto teaches an electroluminescent display, wherein, in operation, the side light output enhancing structure (111) provides areas of different brightness levels (the center region emits light (P1) that is brighter than the light (P3 and P2) emitted at the edges of the pixel) within the display pixel (see Figs. 4(a)-4(b) and paragraph 0051).

Regarding claim 11, the areas are patterned within the pixels providing different brightness levels (see rejection of claim 10, above) and the pixels of the EL display form a display image (the images inherently have different brightness levels since they are formed of pixels having different brightness levels) (see Figs. 4(a)-4(b) and paragraph 0051).

Regarding claim 13, Goto teaches a method of manufacturing an electroluminescent display comprising at least one display pixel, the method at least comprising the steps of: providing a substrate (101); depositing a first electrode layer (109) on or across said substrate (101); depositing an electroluminescent layer (112,113,114) on or across said first electrode layer (109); depositing a second electrode layer (115) on or across said electroluminescent layer (112,113,114), characterized in that said method further comprises a structuring step wherein at least one insulating structure (111) is provided within said display pixel adapted to enhance the light output from said display pixel (for example, see Figs. 4(a)-4(b)).

Regarding claim 14 the structuring step is performed in an insulating layer (111) deposited on or across said first electrode (109) (for example, see paragraph 0047).

Regarding claim 16, Goto teaches the substrate (101) comprising top substrate layers (102,104,106) and the electroluminescent layer comprises emissive layers (112,113,114), the method comprising the step of tuning (selecting) the thickness of the top substrate layers and emissive layers (for example, see paragraphs 0042-0045 and 0048). It is noted that the selection of the thicknesses of the top substrate layers (102,104,106) and the light emitting layers (112,113,114) inherently controls the effects of the light output.

Claims 1, 3, 12, 13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Forrest et al. (US 6,091,195).

Regarding claims 1 and 3, Forrest et al. disclose an electroluminescent display comprising at least one display pixel, said display pixel comprising at least: a substrate (51); a first electrode (26) deposited on or across said substrate (51); an electroluminescent layer (20), and a second electrode (52), characterized in that said display pixel (P) further comprises at least one insulating structure (50), which is part of the substrate (51) as a top substrate layer (50) and is formed within the display pixel so as to enhance the light output from said display pixel (for example, see Figs. 2B and 5A-5E).

Regarding claim 12, Forrest teaches the EL display used in various electronic devices (for example, see col. 12, lines 29-33).

Regarding claim 13, Forrest teaches a method of manufacturing an electroluminescent display comprising at least one display pixel, the method at least comprising the steps of: providing a substrate (60); depositing a first electrode layer (26) on or across said substrate (60); depositing an electroluminescent layer (20) on or across said first electrode layer (26); depositing a second electrode layer (52) on or across said electroluminescent layer (20), characterized in that said method further comprises a structuring step wherein at least one insulating structure (50) is provided within said display pixel adapted to enhance the light output from said display pixel (for example, see Figs. 2B and 2C).

Regarding claim 15, Forrest teaches structuring step being performed in said substrate (60) (for example, see Fig. 2C and col. 7, lines 31-41).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Anthony Perry* whose telephone number is **(571) 272-2459**. The examiner can normally be reached between the hours of 9:00AM to 5:30PM Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. **The fax phone number for this Group is (571) 273-8300.**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Anthony Perry/

Anthony Perry
Patent Examiner
Art Unit 2879
September 25, 2007

NIMESHKUMAR D. PATEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800